



# The OpenDSP Bus

## Electrical and mechanical specifications

*Version 1.0*

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### Introduction

This technical note is concerned with the description of the interface (electrical and mechanical specifications) needed to connect Periphery Boards<sup>1</sup> to the OpenDSP Bus (O-DSP-B) of the OpenDSP System.

### The OpenDSP Bus

The OpenDSP Bus (O-DSP-B) is shown in Figure 1. It is a single master multiple slaves 16-bits parallel bus. Optionally, it can accept a second master, e.g. a Special Communication Board. The bus features a semi-synchronous protocol with four selectable speeds shown in Table 6. In the

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<sup>1</sup> Examples of Periphery Boards are Data Acquisition Boards, Generic digital and analog I/O Boards, PWM Driver Boards, Axes Control Boards.



OpenDSP Mother Board ver. 1.1 (O-DSP-MB1.1), the speed can be selected by means of DIP-switches on the O-DSP-MB1.1 (see [1] for more details).

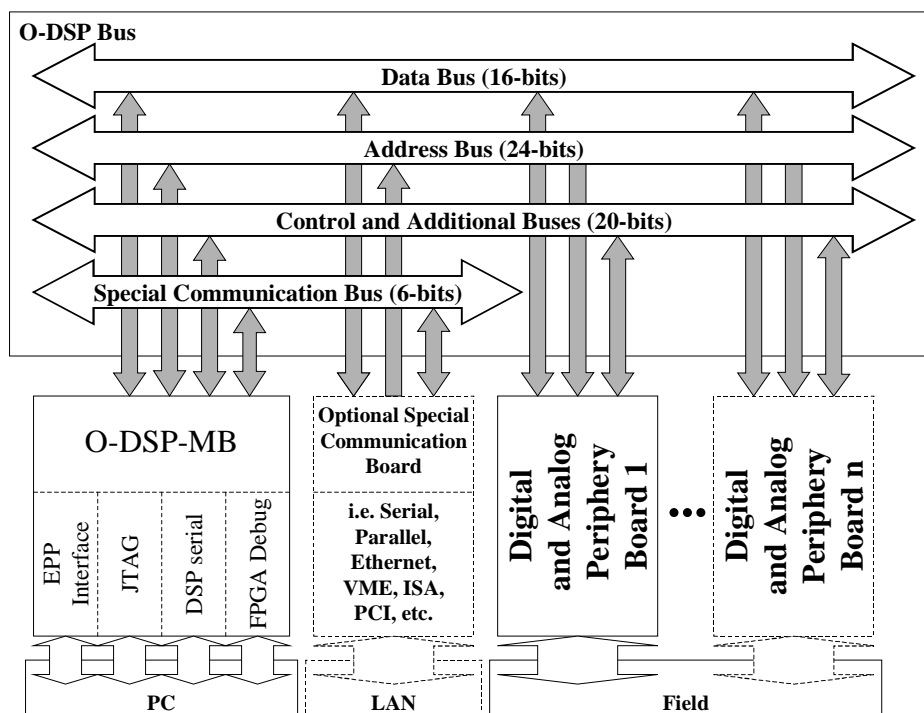


Figure 1 - The OpenDSP System blocks diagram.

The O-DSP-B can be split in five groups of signals:

- **Data Bus** 16 bi-directional lines which represent a data word; all data exchanges among DSP and Periphery Boards are based on 16-bits words;
- **Address Bus** 24 lines corresponding to 16 MWords of address space, of which 3 MWords are reserved to the periphery;
- **Control Bus** 6 lines: ODSPB\_nSTRB1, ODSPB\_nSTRB2, ODSPB\_nSTRB, ODSPB\_R\_nWR, ODSPB\_nWAIT, ODSPB\_nRESET; used to strobe data transfers and reset the system;
- **Special Communication Bus** 6 lines: COM\_nSTRB, COM\_R\_nW, COM\_nHOLD, COM\_nHOLDA, COM\_MSB\_nLSB, COM\_nWAIT; to be used only by the optional Special Communication Board when present;
- **Additional Bus** 14 lines: ODSPB\_TCLK[1..0], ODSPB\_INT[3..2], ODSPB\_nINT[1..0], ODSPB\_IN\_OUT[7..0]; used to synchronize Periphery Boards and to request interrupts to the DSP;
- **Powers Supplies** 3 groups of lines: GND (18 lines), +5V (10 lines), +12V (2 lines).

Details of each O-DSP-B line are shown in Table 1.



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**Table 1** – O-DSP-B lines description. *COM* indicates the Special Communication Bus or Boards.

Signal	Bus	From	To	Note	Description
ODSPB_D[15..0]	Data	Bi-directional		tri-state	Data Bus
ODSPB_A[23..0]	Address	O-DSP-MB	Perip.	tri-state	Address Bus (see the section “Memory map”). This bus is controlled by the O-DSP-MB if the transfer is performed from the O-DSP-B to the Periphery Board (COM_nHOLDA is high) otherwise the bus is controlled by the Communication Board if the transfer is performed from COM to O-DSP-MB or Periphery Boards (COM_nHOLDA is low).
ODSPB_nSTRB1	Control	O-DSP-MB	Perip.		When low strobes a write or read cycle on the Periphery locations from 0x030000 to 0x0303FF (see section “Memory map” for more details). Only the Address Bus Bit0-Bit9 are used.
ODSPB_nSTRB2	Control	O-DSP-MB	Perip.		When low, strobes a write or read cycle on the Periphery locations from 0x040000 to 0x06FFFF (see section “Memory map” for more details). Only the Address Bus Bit0-Bit18 are used.
ODSPB_nSTRB	Control	O-DSP-MB	Perip.		When low strobes a write or read cycle on the total Periphery area (from 0x030000 to 0x3FFFFFF, see the section “Memory map” for more details). Only the Address Bus Bit0-Bit21 are used.
ODSPB_R_nWR	Control	O-DSP-MB	Perip.		When low and ODSPB_nSTRB is low, this signal performs a write cycle on the Periphery Boards. When high and ODSPB_nSTRB is low, a read cycle is performed.
ODSPB_nWAIT	Control	Perip.	O-DSP-MB	pull-up	When low, wait states are added to any write or read cycles.



Table 1 - Cont.

Signal	Bus	From	To	Note	Description
ODSPB_nRESET	Control	O-DSP-MB	Perip.		When low, Periphery Boards must reset. This signal must stay low for at least 3 $\mu$ sec.
ODSPB_TCLK[1..0]	Additional	O-DSP-MB	Perip.		These signals are the outputs of the two DSP internal timers. Typically, rising edge of TCLK[0] is used to synchronize the sampling operations and to trigger changes at periphery outputs (see Figure 4 for an application example), whereas TCLK[1] has no specific function.
ODSPB_INT[3..2]	Additional	Perip.	O-DSP-MB	Pull-up open collector	Programmable active high/low interrupts. When active high, the lines are Wired-AND; when low, the lines are Wired-OR. In the O-DSP-MB1.1, use DIP-SW[6] to program the interrupt level trigger (see Table 4). Typically, ODSPB_INT[2] is set active high to signal End Of Conversion (see Figure 4 for an application example).
ODSPB_nINT[1..0]	Additional	Perip.	O-DSP-MB	pull-up open collector	Wired-OR interrupt requests active low. Typically, when the system runs, ODSPB_nINT[0] indicates errors, abnormal conditions or system alarms from Periphery Boards.
ODSPB_IN_OUT[7..0]	Additional	Bi-directional		pull-up open collector	Programmable inputs (Wired-AND) or outputs. The DSP maps these signals at address 0x020000 of the DSP memory map. Write a byte in the 0x020001 memory location to configure the lines. Meanings are user-defined.



**Table 1 - Cont.**

Signal	Bus	From	To	Note	Description
COM_nSTRB	COM	COM	O-DSP-MB	tri-state	It's high when data transfer are requested by DSP; it's low when data transfer are request by either COM or the O-DSP Host EPP Interface on the O-DSP-MB1.1.
		O-DSP-MB	Perip.		
COM_R_nW	COM	COM	O-DSP-MB		Reserved for Communication Board. Not to be used by Periphery Boards.
COM_nHOLD	COM	COM	O-DSP-MB	Pull-up	Reserved for Communication Board. Not to be used by Periphery Boards.
COM_nHOLDA	COM	O-DSP-MB	COM		Reserved for Communication Board. Not to be used by Periphery Boards.
COM_MSB_nLSB	COM	COM	O-DSP-MB	Pull-up	Reserved for Communication Board. Not to be used by Periphery Boards.
COM_nWAIT	COM	COM	O-DSP-MB	Pull-up	Reserved for Communication Board. Not to be used by Periphery Boards.
GND (18 lines)	Supply				Ground (0 V)
5V (10 lines)	Supply				Power supply (5 V), max 5 A, max 500 mA per pin.
12V (2 lines)	Supply				Power supply (12 V), max 1 A, max 500 mA per pin.

### Timing of Periphery Board accesses to OpenDSP Bus

The timing for O-DSP-B read cycles are shown in Figure 2 and Table 2.

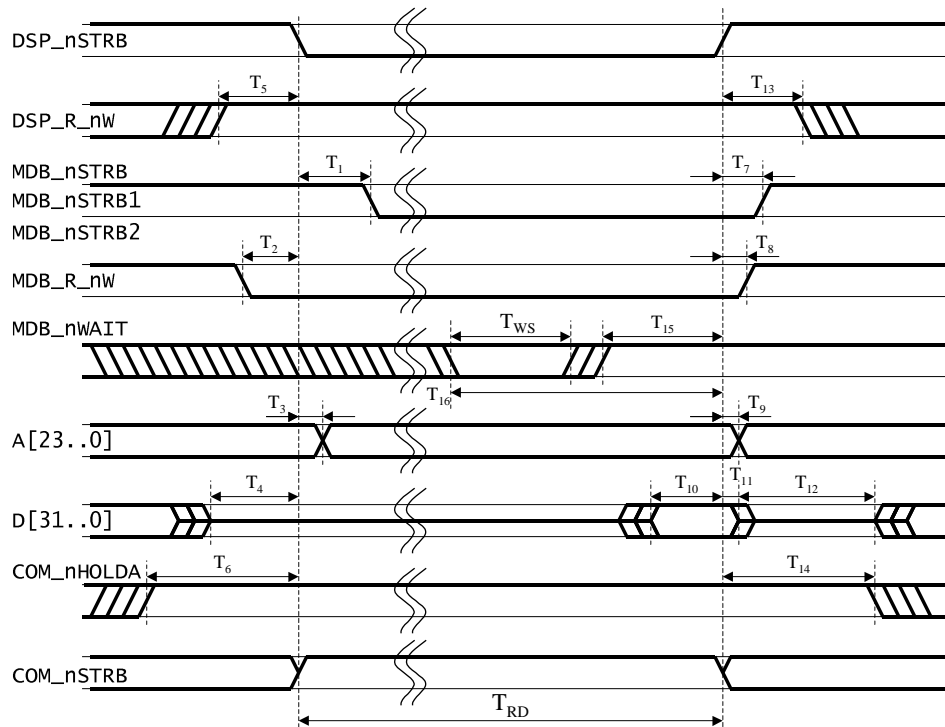


Figure 2 - DSP reading from the Periphery Boards. The times are in Table 2.

Table 2 - Time values corresponding to the O-DSP-B speeds for O-DSP-B read cycle depicted in Figure 2.

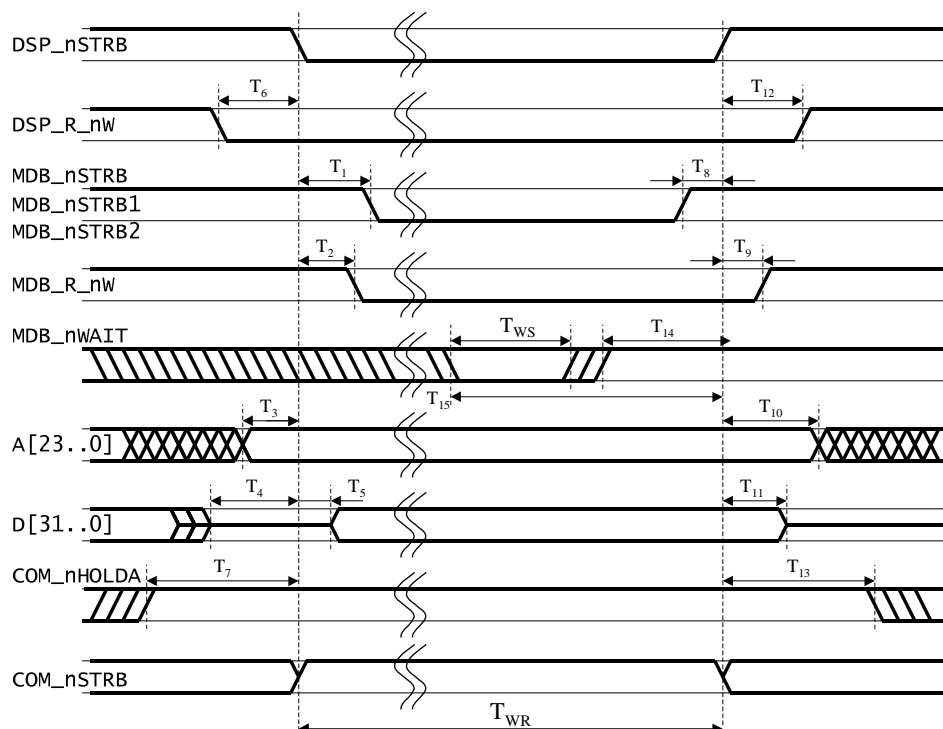
Time		High speed [nsec]	Medium High speed [nsec]	Medium Low speed [nsec]	Low speed [nsec]
T <sub>1</sub>	Min	80	140	200	260
T <sub>2</sub>	Min	44	103	163	224
T <sub>3</sub>	Max	100	160	220	280
T <sub>4</sub>	Min	40	100	160	220
	Max	48	107	167	228
T <sub>5</sub>	Min	65	125	185	245
T <sub>6</sub>	Min	XX	XX	XX	XX
T <sub>7</sub>	Min	60	60	60	60
T <sub>8</sub>	Min	16	16	16	16
T <sub>9</sub>	Min	20	20	20	20
T <sub>10</sub>	Min	40	40	40	40
T <sub>11</sub>	Min	45	45	45	45
T <sub>12</sub>	Min	40	40	40	40

**Table 2 - Cont.**

Time		High speed [nsec]	Medium High speed [nsec]	Medium Low speed [nsec]	Low speed [nsec]
T <sub>13</sub>	Max	20	20	20	20
T <sub>14</sub>	Min	50	50	50	50
T <sub>15</sub>	Min	110	110	110	110
T <sub>RD</sub>		240 + W <sub>S</sub>	420 + W <sub>S</sub>	600 + W <sub>S</sub>	780 + W <sub>S</sub>

$W_S = 60 \cdot \text{Int}(T_{WS}/60)$ ,  $\text{Int}()$  returns the greater integer.

The timing for O-DSP-B write cycles are shown in Figure 3 and Table 3.



**Figure 3 - DSP writing to the Periphery Boards. The times are in Table 3.**



**Table 3** - Time values corresponding to the O-DSP-B speeds for O-DSP-B write cycle depicted in Figure 3.

Time		High speed [nsec]	Medium High speed [nsec]	Medium Low speed [nsec]	Low speed [nsec]
T <sub>1</sub>	Max	28	97	147	208
T <sub>2</sub>	Min	60	120	180	240
	Max	103	162	222	283
T <sub>3</sub>	Max	35	35	35	35
T <sub>4</sub>	Min	40	100	160	220
	Max	38	97	157	218
T <sub>5</sub>	Min	100	160	220	280
T <sub>6</sub>	Min	40	100	160	220
	Max	48	107	147	208
T <sub>7</sub>	Max	160	218	277	335
T <sub>8</sub>	Min	160	220	280	328
	Max	170	228	287	345
T <sub>9</sub>	Min	150	220	270	328
	Max	170	258	317	375
T <sub>10</sub>	Min	190	250	310	358
T <sub>11</sub>	Min	130	190	250	328
	Max	140	198	257	345
T <sub>12</sub>	Min	110	170	230	288
T <sub>13</sub>	Min	40	100	160	238
T <sub>WR</sub>		240 + W <sub>S</sub>	420 + W <sub>S</sub>	600 + W <sub>S</sub>	780 + W <sub>S</sub>

$W_S = 60 \cdot \text{Int}(T_{WS}/60)$ , Int() returns the greater integer.

## Interrupts

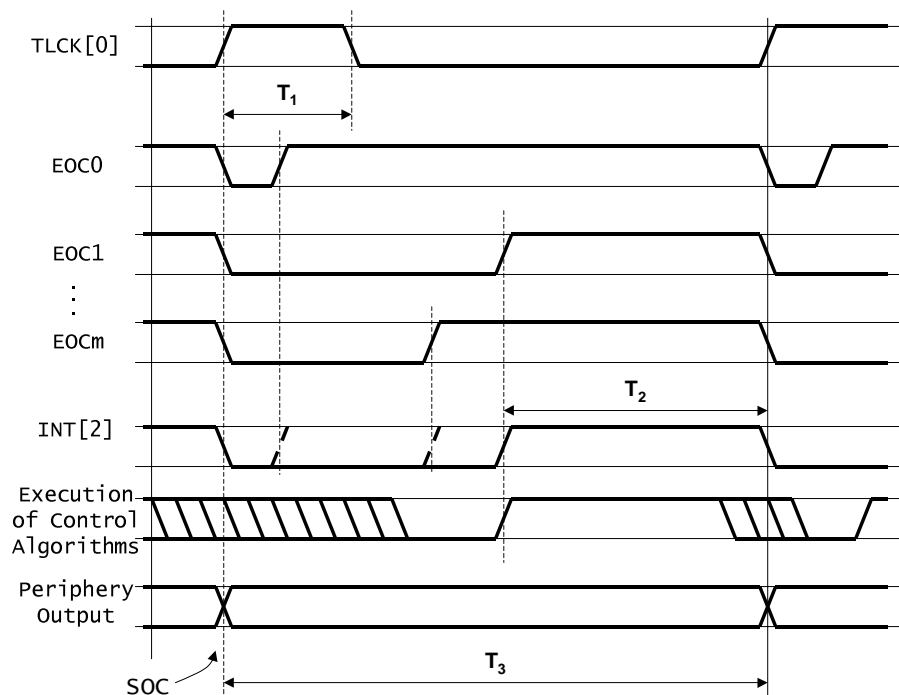
As shown in Table 1, the O-DSP-B has four lines to request interruption to the DSP:

- two interrupts connected in programmable Wired-AND/Wired-OR (ODSPB\_INT[3..2]), corresponding to INT3 and INT2 DSP interrupts;
- two active-low interrupts connected in Wired-OR (ODSPB\_nINT[1..0]), corresponding to INT1 and INT0 DSP interrupts.

In the O-DSP-MB1.1, ODSPB\_INT[3..2] interrupts can be activated with low or high level signals, depending on the DIP\_SW[6]. Table 4 shows the settings.

**Table 4** – DIP\_SW[6] settings.

Interrupt	DIP_SW[0]
ODSPB_INT[3..2] actives low	ON
ODSPB_INT[3..2] actives high (default)	OFF



**Figure 4** - An example of interrupt lines use. The times are in Table 5.

A typical use of the interrupt lines is shown in Figure 4. We suppose there are  $m$  analog-to-digital converters, each one with a different conversion time. When a converter terminates its conversion, it rises its internal EOC (End Of Conversion) signal; when the last converter rises its EOC, the ODSPB\_INT[2] (wired-AND) rises and it signals to the DSP that all conversions are finished. Then, the DSP control algorithm can use the sampled values; in order to preserve overrun errors, the max of the Control Algorithm run time and the conversion times must be less than the sample period. If the Control Algorithms execution run time exceed the end of the period, the outputs are updated in the next period. Notice that the SOC (Start Of Conversion) signal can also trigger the Periphery Board Output transfers. For more information about SOC and EOC generations, see [2].

Table 5 shows the timing corresponding to the four O-DSP-B speeds for applications that use the interrupt lines as described above.



**Table 5** - Time values corresponding to the O-DSP-B speeds for the example of an interrupt use depicted in Figure 4.

Time		High speed [nsec]	Medium High speed [nsec]	Medium Low speed [nsec]	Low speed [nsec]
T <sub>1</sub>	Min	60	120	180	120
T <sub>2</sub>	Min	60	120	180	120
T <sub>3</sub>	Min	180	360	540	720

## General Input/Output

In addition to the interrupt lines, the O-DSP-B has 8 general input/output signals ODSPB\_IN\_OUT[7..0] mapped in the DSP memory space at addresses 0x020000. Signal directions can be programmed writing a byte in the memory space at address 0x020001: Bit0 controls the direction of the ODSPB\_IN\_OUT[0] line, Bit1 controls the direction of the ODSPB\_IN\_OUT[1] line and so on. Set the bits to program the lines as O-DSP-MB outputs, clear the bits to program the lines as O-DSP-MB inputs.

## Electrical specifications

Table 6 shows the DIP-switches configurations used in O-DSP-MB1.1 to select the speed. The O-DSP-MB is always the master of any data exchange, except when the Special Communication Board is given control of the O-DSP-B.

**Table 6** - The OpenDSP System speeds vs. the access source (DSP or O-DSP Host to EPP Interface) and the DIP-switches configurations used in O-DSP-MB1.1 to select the speed. T<sub>H1</sub> indicates the single-cycle instruction execution time (equals to 2/f<sub>CK</sub> and f<sub>CK</sub> is the oscillator clock frequency).

Description	Max Speed to access from DSP	Max Speed to access from O-DSP Host EPP Interface	O-DSP-MB DIP-sw[5..4] configuration
High	1/4T <sub>H1</sub> MW/s	1/5T <sub>H1</sub> MW/s	ON ON
Medium High	1/7T <sub>H1</sub> MW/s	1/8T <sub>H1</sub> MW/s	ON OFF
Medium Low	1/10T <sub>H1</sub> MW/s	1/11T <sub>H1</sub> MW/s	OFF ON
Low	1/13T <sub>H1</sub> MW/s	1/14T <sub>H1</sub> MW/s	OFF OFF

All the O-DSP-B signals are TTL compatible ( $V_{IH\min} = 2\text{ V}$ ,  $I_{IH\max} = 40\text{ }\mu\text{A}$ ,  $V_{IL\max} = 0.8\text{ V}$ ,  $I_{IL\max} = -1.6\text{ mA}$ ,  $V_{OH\min} = 2.4\text{ V}$ ,  $I_{OH\max} = -0.4\text{ mA}$ ,  $V_{OL\max} = 0.4\text{ V}$ ,  $I_{OL\max} = 16\text{ mA}$ ). A complete collection of electrical specifications is shown in Table 7.

The max number of Periphery Boards plugged into the OpenDSP System depends of the selected speed.



Table 7 - Electrical specifications.

Description	High speed	Medium High Speed	Medium Low speed	Low Speed
Max Speed	XXX MHz	YYY MHz	ZZZ MHz	JJJ MHz
Max number of plugged Periphery Board	2	3	4	5
Max O-DSP-B length	XXX m	YYY m	ZZZ m	JJJ m
Max Input Capacitance on each wire (including connectors)	XXX pF			
Min input impedance on each wire	XXX kΩ	YYY kΩ	ZZZ kΩ	JJJ kΩ
Max Powers Supplies Bus Current on each wire	XXX mA			
Max Powers Supplies Bus Total Current	YYY mA			

## Memory map

Figure 5 shows the OpenDSP System memory map. The figure shows also the word sizes.

In detail, each memory area has the following characteristics:

- **memory area from 0x000000 to 0x000FFF** is the 4 Kwords 32-bits DSP internal ROM;
- **memory area from 0x001000 to 0x01FFFF** is a 124 Kwords 8-bits non-volatile RAM (NVRAM); this area is used to store the DSP program and other relevant parameters when power is down; program must start at address 0x001000;
- **memory location 0x020000** (8-bits) this byte is used to map the ODSPB\_IN\_OUT[7..0] signals; writing a value, only lines set as outputs are affected; reading the byte, only lines set as inputs return the read value whereas the lines set as outputs return zero;
- **memory location 0x020001** (8-bits) this byte configures the ODSPB\_IN\_OUT[7..0] signals; Bit0 configures the ODSPB\_IN\_OUT[0] line, Bit1 configures the ODSPB\_IN\_OUT[1] line and so on; set the bit to configure the line as an output, clear the bit to configure it as an input;
- **memory location 0x020002** (8-bits) the O-DSP Host EPP Interface requests PC interruption when Bit0 is set; the O-DSP Host EPP Interface falls the interrupt line if the Bit0 is cleared;
- **memory location 0x020003** (8-bits) contains information about the SRAM memory chips installed on the O-DSP-MB; the nibbles meanings are shown in Table 8 and Table 9;
- **memory location 0x020004** (8-bits) contains the O-DSP-MB version; the nibbles meanings are shown in Table 10;

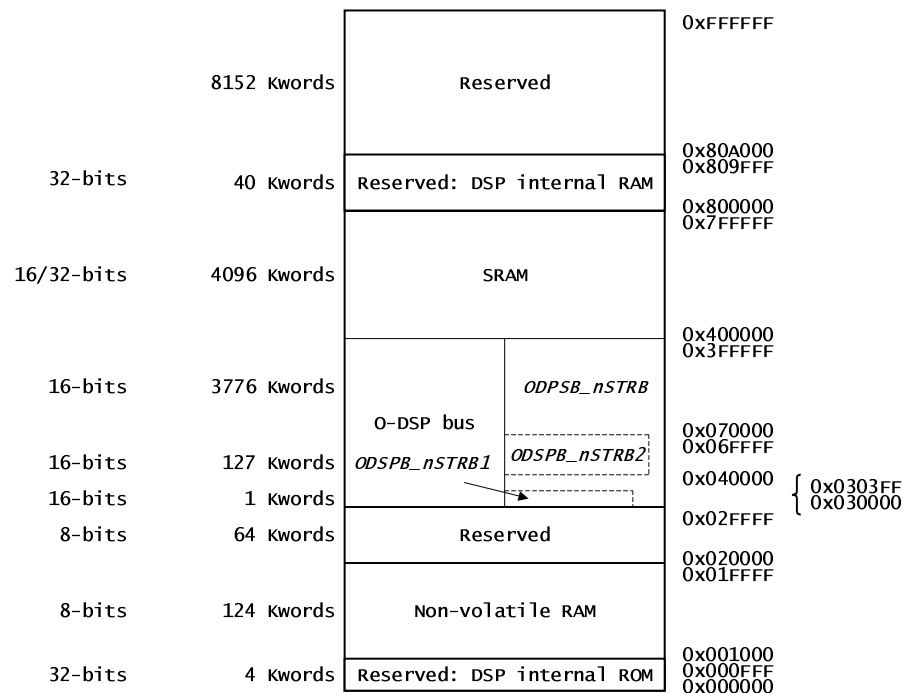


Figure 5 - The OpenDSP System memory map.

- **memory location 0x020005** (8-bits) this location corresponds to the register to mask the interruption of INT2 and INT3; after the reset, these interrupts are disabled. Set Bit0 to enable the interruption on the INT2 and INT3 line;
- **memory location 0x020006** (8-bits) this location is the initial value of the watch-dog counter;
- **memory location 0x020007** (8-bits) a write operation on this location initializes the watch-dog counter with the value stored in the 0x020006 location;
- **memory area from 0x020008 to 0x02FFFF** (8-bits) this area is reserved;
- **memory area from 0x030000 to 0x3FFFFF** this area is a 3904 Kwords 16-bits memory; this area is used to map Periphery Boards; the entire memory area is accessed when ODSPB\_nSTRB is low; the memory area from 0x040000 to 0x06FFFF is accessed when ODSPB\_nSTRB and ODSPB\_nSTRB2 are low; the memory area from 0x030000 to 0x0303FF is accessed when ODSPB\_nSTRB and ODSPB\_nSTRB1 are low;
- **memory area from 0x400000 to 0x7FFFFF** this area is a 32-bits O-DSP-MB RAM; different SRAM memory chips combinations are actually supported (64K, 256K, 1024K, 4096K);
- **memory area from 0x800000 to 0x809FFF** this area is the 40 Kwords 32-bits DSP internal RAM;
- **memory area from 0x80A000 to 0xFFFFF** this area is reserved.



**Table 8** - The bits meanings of the memory location mapped in 0x020003.

0x020003 location bits	Description
From Bit0 to Bit3	Contains the coding (see Table 9) of the SRAM chip plugged into the first slot (named ZIP1 in the O-DSP-MB1.1 layout)
From Bit4 to Bit7	Contains the coding (see Table 9) of the SRAM chip plugged into the second slot (named ZIP2 in the O-DSP-MB1.1 layout)

**Table 9** - SRAM chip coding.

SRAM chip coding	Description
D	64 Kwords
B	256 Kwords
A	1024 Kwords
F	No chip

**Table 10** - The bits meanings of the memory location mapped in 0x020004.

0x020004 location bits	Description
From Bit0 to Bit3	Contains the O-DSP-MB minor version number
From Bit4 to Bit7	Contains the O-DSP-MB major version number

## The Boards mechanical specifications

Table 11 shows the mechanical specifications for Boards pluggable into the OpenDSP System. Figure 6 shows the layout of the O-DSP-MB as example; the positions of the drills and the dimensions are also shown. Figure 7 shows the Terminations Boards dimensions and the positions of the drills.

The O-DSP-B can be realized using either a Back Plane or a flat cable. When a flat cable is used, Adapter Boards are needed. Figure 8 shows the Adapter Board dimensions and the position of the drills.

Figure 9 shows an example of Back Plane. It can connect eight Boards (one O-DSP-MB and seven Periphery Boards or one O-DSP-MB, one Special Communication Board and six Periphery Boards). The Back Plane dimensions and the positions of the drills are also depicted.



Table 11 - Mechanical specifications.

Description	Details
Boards type	Half Eurocard
Boards sizes (see Figure 6)	160.0 mm x 100.3 mm (6300 mils x 3950 mils)
Boards to O-DSP-B connector	96 pins male – DIN96 - 90°
O-DSP-MB to EPP connector	26 pins male – standard flat connector
O-DSP-MB to Serial Port connector	12 pins male – standard flat connector
O-DSP-MB to TI scan connector	12 pins male – standard flat connector
O-DSP-MB to Altera connector	10 pins male – standard flat connector
O-DSP Boards to Backplane or Flat Adapter connectors	96 pins male – DIN96 - 90°
Termination Boards to Backplane or Flat Adapter connectors	96 pins male – DIN96
Termination Boards sizes (see Figure 7)	61.0 mm x 100.3 mm (2400 mils x 3950 mils) with RC-loads
Flat Adapter Board sizes (see Figure 8)	54.6 mm x 100.3 mm (2150 mils x 3950 mils)

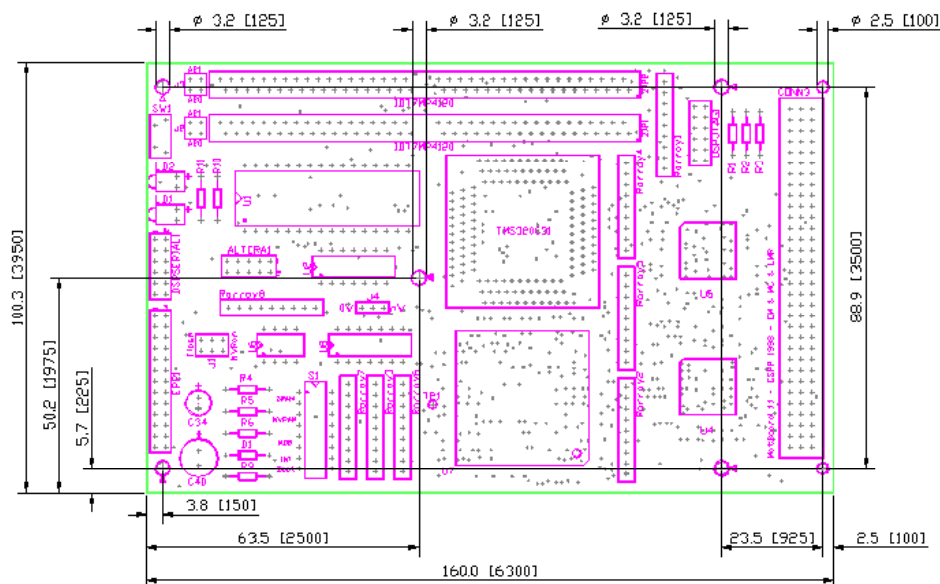
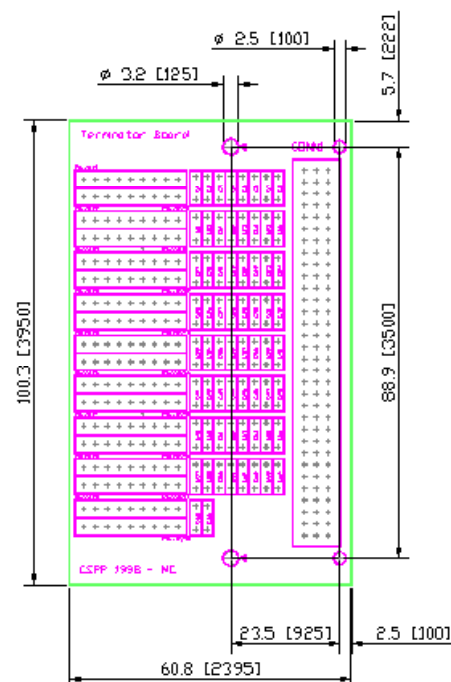
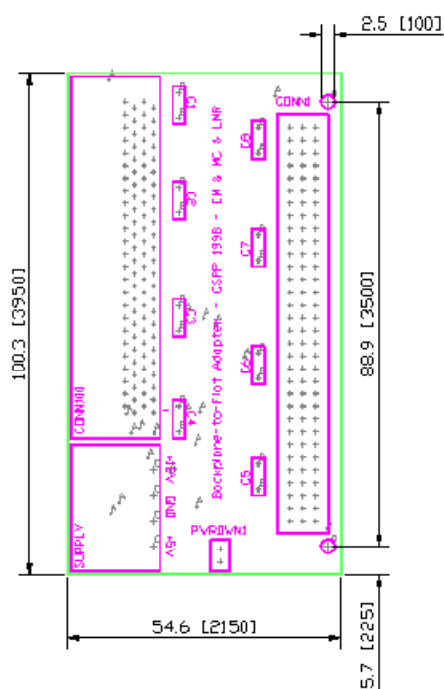
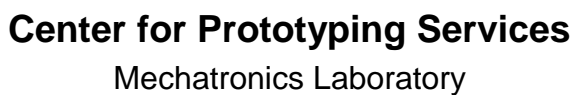
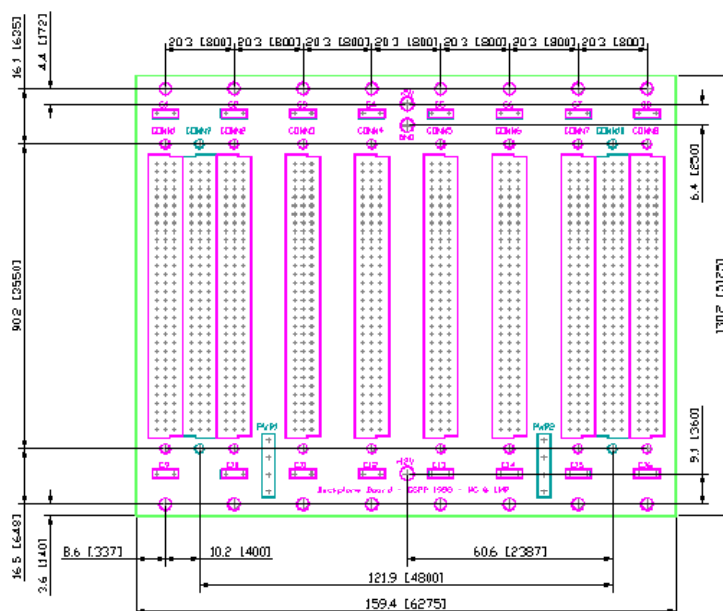
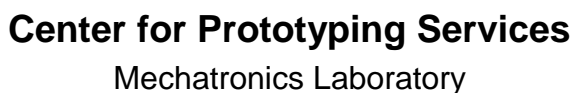


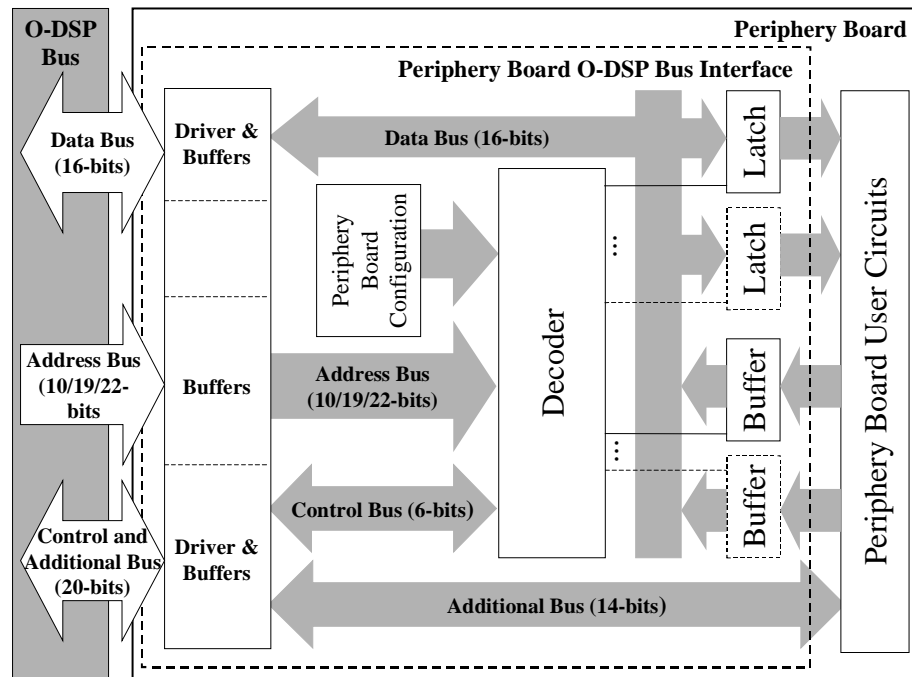
Figure 6 - The dimensions and the drills positions of the O-DSP-MB1.1 and Periphery Boards. The dimensions are in mm (mils in brackets).



**Figure 7** - The dimensions and the drills positions of the OpenDSP Termination Board ver. 1.1. The Termination Board has capacitive and resistive loads. The dimensions are in mm (mils in brackets).







**Figure 10** - Block scheme of the Periphery Board O-DSP-B Interface.

According to the address space required by the Periphery Board, the interface can decode specific O-DSP-B lines. If the Periphery Board requires less than 100 addresses, it can be mapped between address 0x030000 and 0x0303FF; ODSPB\_nSTRB1 and ODSPB\_A[9..0] are sufficient to decode the addresses. If the Periphery Board requires more than 100 addresses but less than 10 thousand of addresses, it can be mapped between the address 0x040000 and 0x06FFFF; ODSPB\_nSTRB2 and ODSPB\_A[18..0] are sufficient. If the Periphery Board requires more than 10 thousand of addresses, it can be mapped between the address 0x070000 and 0x3FFFFF; ODSPB\_nSTRB and ODSPB\_A[21..0] must be used.

## Bibliography

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- [2] E. Miranda and M. Chiaberge, "The OpenDSP General Purpose I/O ver. 1.1", Politecnico di Torino, 1998

## Related documents

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- A.A.V.V., "Application Notes", Politecnico di Torino, 1998