



# MatDSP 3.2 for OpenDSP System Notes

*Version 1.0*

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## Introduction

This document describes the special features of MatDSP ver. 3.2 for the OpenDSP System (see [1]).

MatDSP 3.2 is completely equivalent, and almost completely code compatible, to the previous version MatDSP 3.1, therefore refer to the MatDSP 3.1 documentation.

**IMPORTANT NOTE:** the main difference with respect to the MatDSP 3.1 software and related documentation concerns the file name extensions: MatDSP 3.2 source and header files extensions are simply `.c` and `.h`, instead of `.c3x` and `.h3x`. In particular, all the MatDSP 3.1 user files must include `matdsp.h` instead of `matdsp.h3x`. Moreover, to use the old user files, some configuration for the I/O channels are required, those are described in the following.

The new user files, created by means of the `dspnew` command do not need any change.

## OpenDSP System

OpenDSP System, in its basic configuration, consists of a DSP Mother Board (O-DSP-MB1.1), a General Purpose I/O Board (O-DSP-IO1.1) (for more details see [2], [3] and

[5]) and a Backplane Board (O-DSP-BB1.1), hosted in a separate box, whose front panel carries the EPP as well as the I/O connectors (see Figure 1).



**Figure 1** - OpenDSP System Box

## MatDSP 3.2 in command mode

MatDSP 3.2 behaves exactly in the same way as the previous version MatDSP 3.1, except in the number of I/O channels. Actually, the OpenDSP system has, in its basic configuration, 8 analog input and 8 analog output channels. Since the number of enabled input channels influences the maximum achievable sampling frequency, the functions available in the MatDSP toolbox, that are used in the command mode, have been pre-compiled with a specific number of input channels, reported in Table 1 (both the Matlab commands and the correspondent DSP source files are listed). The user should only be aware of the number of analog I/O channels effectively enabled, for each pre-compiled function available in the toolbox.

**Table 1** - Number of channels enabled in the functions available in the MatDSP toolbox.

Matlab toolbox command	Number of enabled analog input channels	DSP source code
<b>dspacq</b>	4	acquire, acquiret
<b>dspiir</b>	1	dspiir
<b>dspiirc</b>	1	dspiirq



Table 1- Cont.

Matlab toolbox command	Number of enabled analog input channels	DSP source code
<b>dspiirn</b>	1	dspiirn
<b>dsppid</b>	1	dsppid
<b>dsppidc</b>	1	dsppidq
<b>dspsgen</b>	4	dspsgen
<b>dspss</b>	4	dspss, dspssd, dspssj
<b>dspssc</b>	4	dspssq, dspssq2
<b>dsptest</b>	8	echo
<b>dspzero</b>	8	dspzero

## MatDSP 3.2 in programming mode

### OpenDSP Mother Board ver. 1.1 registers and constants

MatDSP 3.2 provides some configuration registers and constants to enable the INT2 and INT3 generation.

The available functions and macros are listed in **Table 2**.

**Table 2** - OpenDSP Mother Board 1.1 registers.

Registers and constants	Description
EnableINT23	register to enable the interrupt request from the OpenDSP Bus. Set Bit0 to enable the interruption on the INT2 and INT3 line. After the reset, these interrupts are disabled.
ENABLE_ODSPB_INT23	constant to enable the INT2 and INT3
DISABLE_ODSPB_INT23	constant to disable the INT2 and INT3

### OpenDSP General Purpose I/O ver. 1.1 macros

MatDSP 3.2 provides some macros to configure the O-DSP-IO1.1 A/D channels. The configuration macros allow to enable and to set the input range, independently for each A/D channel (see file IOBOARD.H).

The available functions and macros are listed in Table 3.



**Table 3** – Functions and macros to configure the OpenDSP General Purpose I/O Board ver. 1.1.

Function or macro	Description
<code>IOBoardInit()</code>	I/O initialization in line function; this function initializes the <code>fADweight[ch]</code> bit to mV A/D conversion factors, the <code>_IOBOARD_gain_[ch]</code> and the <code>_IOBOARD_sat_[ch]</code> arrays
<code>config_ad(ch,range,bipolar)</code> <sup>1</sup>	enables and configures the A/D channel <code>ch</code>

## Advanced programming mode

In this section advanced programming notes are described.

### DSP software architecture

The DSP code architecture of MatDSP 3.2 is composed of a main program calling a number of subroutines. The user is provided with a simple interface (in the form of a single template file) to the part of the code that may be customized (see [6]).

Accordingly to the default on-board DIP-switches configuration (see [5]), the Timer 1 rising edge generates the Start of Conversion for the General Purpose I/O Board enabled analog channels. When all of channels have been converted the End of Conversion generates the interrupt 2 request to the DSP. Therefore the correspondent ISR `c_int03()` is executed at every cycle; inside this ISR the `user_ctrl()` routine is called (see [6]).

The interrupt 3 is used to allow the user to stop and restart the DSP code; the correspondent ISR is `c_int04()`. Into this ISR, the `user_stop()` and `user_restart()` routines are called (see [6]).

It is important to note that at least one analog input channel must be enabled, in order to execute the `c_int03` (and therefore the `user_ctrl()`).

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<sup>1</sup> Possible values for the input arguments are:

`ch = 0, 1, 2, 3, 4, 5, 6, 7;`

`range = IO_CH0_10V, IO_CH1_10V, IO_CH2_10V, IO_CH3_10V, IO_CH4_10V, IO_CH5_10V, IO_CH6_10V, IO_CH7_10V, IO_CH0_5V, IO_CH1_5V, IO_CH2_5V, IO_CH3_5V, IO_CH4_5V, IO_CH5_5V, IO_CH6_5V, IO_CH7_5V;`

`bipolar = IO_CH0_BIPOLAR, IO_CH1_BIPOLAR, IO_CH2_BIPOLAR, IO_CH3_BIPOLAR, IO_CH4_BIPOLAR, IO_CH5_BIPOLAR, IO_CH6_BIPOLAR, IO_CH7_BIPOLAR, IO_CH0_UNIPOLAR, IO_CH1_UNIPOLAR, IO_CH2_UNIPOLAR, IO_CH3_UNIPOLAR, IO_CH4_UNIPOLAR, IO_CH5_UNIPOLAR, IO_CH6_UNIPOLAR, IO_CH7_UNIPOLAR.`



## OpenDSP Mother Board ver. 1.1 registers

In order to allow the O-DSP-MB1.1 software configuration, some unsigned 32-bit variables are defined (see file ODSPMB11.H and [4]), listed in Table 4.

**Table 4** – OpenDSP Mother Board 1.1 registers.

Registers	Description
AlteraAuxIOConf	OpenDSP Bus additional I/O programmable signals configuration. Bit0 configures the ODSPB_IN_OUT[0] line, Bit1 configures the ODSPB_IN_OUT[1] line and so on; set the bit to configure the line as an output, clear the bit to configure it as an input;
AlteraAuxIO	OpenDSP Bus additional I/O programmable signals. Writing a value, only lines set as outputs are affected; reading the byte, only lines set as inputs return the read value whereas the lines set as outputs return zero;

## OpenDSP General Purpose I/O ver. 1.1 macros

MatDSP 3.2 provides some macros to configure the O-DSP-IO1.1 A/D channels. The configuration macros allow to enable and to set the input range, independently for each A/D channel (see file IOBOARD.H).

The available functions and macros are listed in Table 5.

**Table 5** - Macros to configure the OpenDSP General Purpose I/O Board ver. 1.1.

Function or macro	Description
SEL_CONF_ADC(ch,range,bidir)	A/D selection and configuration macro
IS_ADC_ENABLED(ch)	enabled A/D channel boolean value
IS_ADC_10V(ch)	range A/D channel boolean value
IS_ADC_BIPOLAR(ch)	bipolar configuration A/D channel boolean value
IOBOARD_READ_AD_MV(ch)	writes the converted value in mV in IOBOARD_AD_MV[ch]
IOBOARD_READ_AD_BIT(ch)	writes the converted value in bits in IOBOARD_AD_BIT[ch]
IOBOARD_WRITE_DA_MV(ch)	writes the value in mV onto the D/A channel ch
IOBOARD_WRITE_DA_BIT(ch)	writes the value in bits onto the D/A channel ch



**Table 5** – Cont.

Function or macro	Description
IOBOARD_OUT_CH_S(ch,outval)	writes the value in mV, with saturation, onto the D/A channel ch
IOBOARD_OUT_CH_GS(ch,outval)	writes the value in mV, multiplied by the gain and with saturation, onto the D/A channel ch

### OpenDSP General Purpose I/O ver. 1.1 registers, constants and variables

MatDSP 3.2 provides some specific memory-mapped registers, constants and variables for the O-DSP-IO1.1, that are listed in Table 6 (see files IOBOARD.H and PERIPHER.H).

**Table 6** – OpenDSP General Purpose I/O Board ver. 1.1 registers, costants and variables.

Registers, constants and variables	Description
IOBOARD_NO_AD	number of A/D channels
IOBOARD_NO_DA	number of D/A channels
IOBOARD_OUTPUT_MAX_MV	maximum D/A output value in mV
IOBOARD_MV2BIT	mV to bit conversion constant
IOBOARD_ch[ch]	analog channels
_IOBOARD_gain_[ch]	analog channels gains
_IOBOARD_sat_[ch]	analog channels saturation levels
IOBOARD_AD_MV[ch]	A/D channels in mV
IOBOARD_AD_BIT[ch]	A/D channels in bits
IOBOARD_DA_MV[ch]	D/A channels in mV
IOBOARD_DA_BIT[ch]	D/A channels in bits
IO1_ADC_DAC_CH0	analog channel number 0 (input if read, output if written);
IO1_ADC_DAC_CH1	analog channel number 1, (input if read, output if written);
IO1_ADC_DAC_CH2	analog channel number 2, (input if read, output if written);
IO1_ADC_DAC_CH3	analog channel number 3, (input if read, output if written);
IO1_ADC_DAC_CH4	analog channel number 4, (input if read, output if written);
IO1_ADC_DAC_CH5	analog channel number 5, (input if read, output if written);



**Table 6 - Cont.**

<b>Registers, constants and variables</b>	<b>Description</b>
IO1_ADC_DAC_CH6	analog channel number 6, (input if read, output if written);
IO1_ADC_DAC_CH7	analog channel number 7, (input if read, output if written);
IO1_DIG_LSW	digital I/O lower 16 bits (the value written is sent to the DIGOUT connector, the value read correspond to the signals on the DIGIN connector);
IO1_DIG_MSW	digital I/O upper 16 bits (the value written is sent to the DIGOUT connector, the value read correspond to the signals on the DIGIN connector);
IO1_ENABLE_REG	analog channels enable register; set Bit0 to enable channel 0, set Bit1 to enable channel 1 and so on;
IO1_CONFIG_REG	analog channels input range configuration register. Bit0 configures the ADC channel 0 max. input value, Bit1 configures the ADC channel 1 max. input value and so on. Set the bit to set the channel 0 max. input value to 10 V; clear it to set the channel 1 max. input value to 5 V. Bit8 configures the ADC channel 0 input range, Bit9 configures the ADC channel 1 input range and so on. Set the bit to set the channel range bipolar, clear it to set the channel range no-bipolar.
IO1_SOC_REG	start of conversion (SOC) register; set Bit0 to set the DAC SOC, set Bit1 to set the ADC SOC; read Bit0 to detect the ADC EOC.

The O-DSP-IO1.1 can be mapped into several DSP memory addresses, depending on its on-board DIP-switches configuration (see [3]). In the default configuration (see [5]), the addresses listed in Table 7 are selected.



**Table 7** - OpenDSP General Purpose I/O Board ver 1.1 default address configurations.

Constant	Address
IO1_ADC_DAC_CH0_C	0x030010
IO1_ADC_DAC_CH1_C	0x030011
IO1_ADC_DAC_CH2_C	0x030012
IO1_ADC_DAC_CH3_C	0x030013
IO1_ADC_DAC_CH4_C	0x030014
IO1_ADC_DAC_CH5_C	0x030015
IO1_ADC_DAC_CH6_C	0x030016
IO1_ADC_DAC_CH7_C	0x030017
IO1_DIG_LSW	0x030018
IO1_DIG_MSW	0x030019
IO1_ENABLE_REG	0x03001A
IO1_CONFIG_REG	0x03001B
IO1_SOC_REG	0x03001C

## DSP on-chip peripherals

MatDSP 3.2 gives the user access to the on-chip DSP peripherals (two timers and one serial port, see [7]) by providing the correspondent memory-mapped registers as 32-bit unsigned integer variables directly addressable in the C environment. These registers are listed in Table 8 (see file MEMREGS.H).

**Table 8** - On-chip DSP peripherals registers.

Memory-mapped register	Description
Tim0GlobCtrl	Timer 0 Global Control Register
Tim0Cntr	Timer 0 Counter Register
Tim0Prd	Timer 0 Period Register
Tim1GlobCtrl	Timer 1 Global Control Register
Tim1Cntr	Timer 1 Counter Register
Tim1Prd	Timer 1 Period Register
SerGlobCtrl	Serial Port Global Control Register
XportCtrl	FSX/DX/CLKX Port Control Register
RportCtrl	FSR/DR/CLKR Port Control Register



**Table 8** – Cont.

<b>Memory-mapped register</b>	<b>Description</b>
RXTimCtrl	R/X Timer Control Register
RXTimCntr	R/X Timer Counter Register
RXTimPrd	R/X Timer Period Register
DataTx	Data Transmit Register
DataRx	Data Receive Register



## Bibliography

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