



# OpenDSP System - Description and Tests

Version 1.0

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## Introduction

This document describes the OpenDSP System installed components, the connectors pins, the system configuration, the default DIP-switches settings and the performed tests for the specific customer system.

The section “System Components” lists the plugged boards and power supply contained into the box. The system is equipped with the checked components only.



The section “Front and Back Panels” lists the switches, fuses, LEDs, buttons and connectors available on the front and back panels. The system is equipped with the checked components only.

The section “Connectors” lists the pin assignment for each connector.

The section “System configuration and default DIP-switches settings” lists the oscillator and jumpers configuration and the default DIP-switches settings.

The section “Tests” lists the tests performed during the system assembling. The list reports the purpose, the date, the operator and the results for each test.

## System Components

The OpenDSP System consists of:

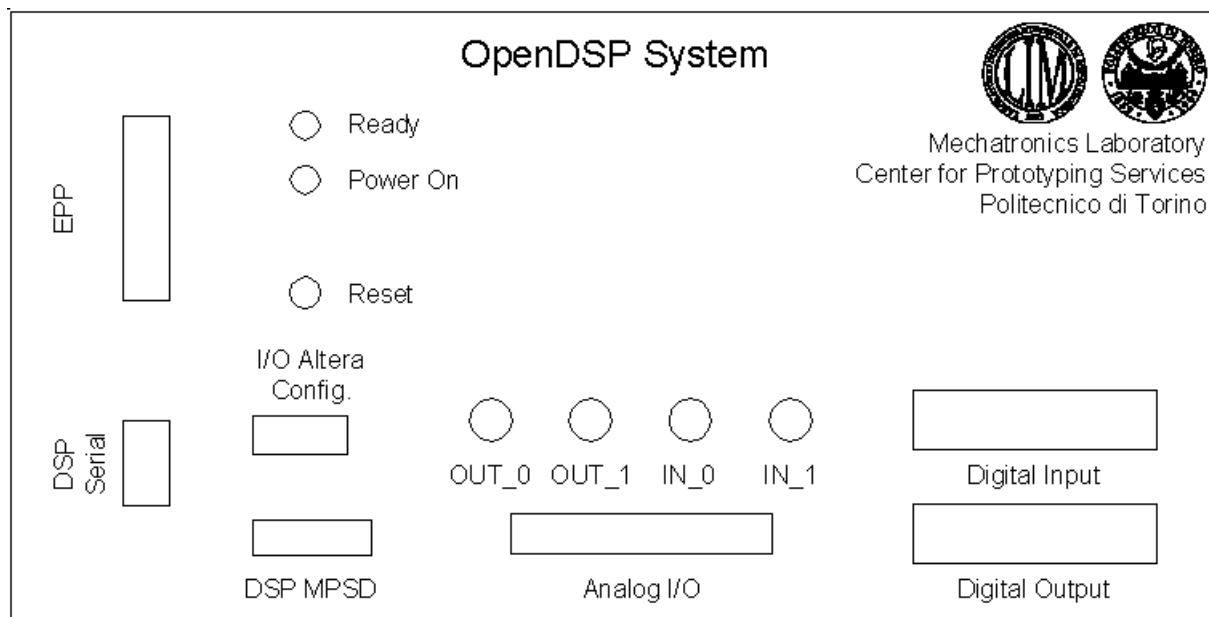
- ☒ OpenDSP Mother Board ver. 1.1 (O-DSP-MB1.1), no. 5
- ☒ OpenDSP General Purpose I/O Board ver. 1.1 (O-DSP-IO1.1), no. 5
- ☒ OpenDSP Backplane Board ver. 1.1 (O-DSP-BB1.1), no. 5
- ☐ OpenDSP Flat Adapter Board ver. 1.1 (O-DSP-FA1.1), no.
- ☐ OpenDSP Termination Board ver. 1.1 (O-DSP-TB1.1), no.
- ☐ OpenDSP Termination Board ver. 1.2 (O-DSP-TB1.2), no.

The OpenDSP System is provided in a box containing also a power supply unit (input: 220÷240 VAC, 50÷60 Hz; output: 5 V, 12 V, –12 V).

## Front and Back Panels

The OpenDSP System front panel is showed in Figure 1. Onto the front panel there are:

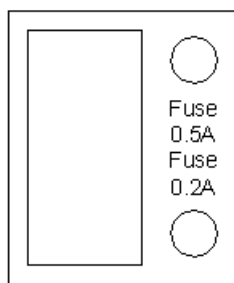
- ☒ **EPP D25-pin male connector:** OpenDSP System to host PC connection by means of an Enhanced Parallel Port (EPP, see [1] and [2] for more details);
- ☒ **DSP Serial D15-pin male connector:** connector to allow the use of the DSP serial port (see [3]); this connector is present only if the customer requests it;
- ☒ **Power On green led:** DSP Mother Board power on; it switches on when the DSP Mother Board is supplied with the 5 V;
- ☒ **Ready red led:** DSP Mother Board FPGA ready; it switches on immediately after the green led, when the DSP Mother Board FPGA has been configured;
- ☒ **Reset push button:** OpenDSP System reset;
- ☒ **I/O Altera Config. PCB male 10-pin connector:** port to configure the I/O Board FPGA. To configure the FPGA it is necessary to use a downloader program as that integrated into the Altera Max Plus II ver. 8.2 and a programmer cable as the Altera BitBlaster (see [4] for more details). IMPORTANT NOTE: the system is provided with a configuration EPROM for this FPGA; the I/O Altera Config. connector must not be connected when the EPROM is onto its socket.



**Figure 1** - The OpenDSP System front panel. The DSP Serial connector is present only by request.

- ☑ **DSP MPSD PCB male 14-pin connector:** Texas Instruments emulation Modular Port Scan Device (MPSD); it allows the connection with a XDS-510 interface;
- ☑ **Analog I/O D37-pin female connector:** I/O Board analog input and output; it makes available the I/O Board analog 8 inputs and 8 outputs;
- ☑ **OUT\_0, OUT\_1, IN\_0, IN\_1 BNC connectors:** I/O Board analog input channel 0 and channel 1, analog output channel 0 and channel 1;
- ☑ **Digital Input D50-pin female connector:** I/O Board 32 digital input pins;
- ☑ **Digital Output D50-pin female connector:** I/O Board 32 digital output pins.

Both the switch and the power supply are provided with a 2.5 A 250 V fuse; the switch fuse is externally accessible on the back panel (see Figure 2). Two overcurrent protection fuses are also provided for the DC power supplies accessible on the back panel (one 500 mA 250 V fuse for the 5 V and one 200 mA 250 V fuse for the 12 V).



**Figure 2** - The OpenDSP System back panel.



## Connectors

### Digital Input and Digital Output Connectors

Table 1 shows the pinout for the Digital Input and Digital Output connectors.

**Table 1** - Digital Input and Digital Output connectors pin assignment.

Pin number	Description	Pin number	Description
1	DATA_16	26	GND
2	DATA_0	27	DATA_9
3	DATA_18	28	GND
4	DATA_2	29	DATA_11
5	DATA_20	30	GND
6	DATA_4	31	DATA_13
7	DATA_22	32	GND
8	DATA_6	33	DATA_15
9	GND	34	GND
10	DATA_8	35	GND
11	DATA_25	36	GND
12	DATA_10	37	GND
13	DATA_27	38	GND
14	DATA_12	39	GND
15	DATA_29	40	GND
16	DATA_14	41	GND
17	DATA_31	42	GND
18	DATA_17	43	DATA_24
19	DATA_1	44	GND
20	DATA_19	45	DATA_26
21	DATA_3	46	GND
22	DATA_21	47	DATA_28
23	DATA_5	48	GND
24	DATA_23	49	DATA_30
25	DATA_7	50	GND

### Analog I/O Connector

Table 2 shows the pinout for the Analog I/O connector.

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**Table 2** - Analog I/O connector pin assignment.

Pin number	Description	Pin number	Description
1	GND	20	IN_CH0
2	IN_CH1	21	GND
3	GND	22	IN_CH2
4	IN_CH3	23	GND
5	GND	24	IN_CH4
6	IN_CH5	25	GND
7	GND	26	IN_CH6
8	IN_CH7	27	GND
9	GND	28	VCC
10	VCC	29	OUT_CH0
11	OUT_CH1	30	GND
12	GND	31	OUT_CH2
13	OUT_CH3	32	GND
14	GND	33	OUT_CH4
15	OUT_CH5	34	GND
16	GND	35	OUT_CH6
17	OUT_CH7	36	GND
18	Not connected	37	Not connected
19	Not connected		

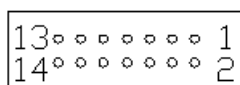
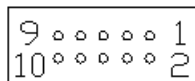
### Altera I/O Config. Connector

Table 3 shows the pinout for the Altera I/O Config. connector. The Figure 3 shows the connector pin numbers.

**Table 3** – Altera I/O Config. connector pin assignment.

Pin number	Description	Pin number	Description
1	GND	6	NCONFIG
2	DATA	7	VCC
3	Not connected	8	CONF_DONE
4	NSTATUS	9	GND
5	Not connected	10	DCLK

## I/O Altera Config.



## DSP MPSD

**Figure 3** - I/O Altera Config. and DSP MPSD connectors with pin numbers.

## EPP Connector

Table 4 shows the pinout for the EPP connector.

**Table 4** - EPP connector pin assignment.

Pin number	Description	Pin number	Description
1	NWRITE	14	NDSTRB
2	DATA_0	15	SPARE_2
3	DATA_1	16	Not connected
4	DATA_2	17	NASTRB
5	DATA_3	18	NALARM
6	DATA_4	19	GND
7	DATA_5	20	GND
8	DATA_6	21	GND
9	DATA_7	22	GND
10	INT	23	GND
11	NWAIT	24	GND
12	SPARE_0	25	GND
13	SPARE_1		



## DSP MPSD Connector

Table 5 shows the pinout for the DSP MPSD connector. The Figure 3 shows the connector pin numbers.

**Table 5** - DSP MPSD connector pin assignment.

Pin number	Description	Pin number	Description
1	Not connected	8	VCC
2	Not connected	9	GND
3	GND	10	EMU2
4	H3	11	GND
5	GND	12	EMU0
6	EMU3	13	GND
7	No pin (key)	14	EMU1

## DSP Serial Connector

Table 6 shows the pinout for the DSP Serial connector.

**Table 6** - DSP Serial connector pin assignment.

Pin number	Description	Pin number	Description
1	CLKX0	9	FSX0
2	CLKR0	10	GND
3	MDB_nINT0	11	XF1
4	MDB_nINT1	12	XF0
5	DR0	13	Not connected
6	GND	14	Not connected
7	DX0	15	Not connected
8	FSR0		

## System configuration and default DIP-switches settings

The OpenDSP System configuration and the default DIP-switches settings are listed in the following tables.

### DSP Mother Board system configuration

Table 7 shows the DSP Mother Board (O-DSP-MB1.1) system configuration. For more details see reference [5].



**Table 7** - The OpenDSP Mother Board ver. 1.1 system configuration.

Quartz oscillator (U2)	25.175 MHz
Wait States Jumper (J4)	0 W
NVRAM/Flash Jumpers (J1)	NVRAM

### DSP Mother Board default DIP-switches settings

Table 8 shows the DSP Mother Board (O-DSP-MB1.1) default DIP-switches settings. For more details see reference [5].

**Table 8** - The OpenDSP Mother Board ver. 1.1 default DIP-switches settings.

Switch S1	Default setting
1 (SRAM)	ON
2 (SRAM)	ON
3 (NVRAM)	OFF
4 (NVRAM)	OFF
5 (MDB)	ON
6 (MDB)	ON
7 (INT)	OFF
8 (Boot)	ON

### General Purpose I/O Board system configuration

Table 9 shows the General Purpose I/O Board (O-DSP-IO1.1) system configuration. For more details see reference [6].

**Table 9** - The OpenDSP General Purpose I/O ver. 1.1 system configuration.

Quartz oscillator (U6)	8 MHz
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### General Purpose I/O Board default DIP-switches settings

Table 10 shows the General purpose I/O Board (O-DSP-IO1.1) default DIP-switches settings. For more details see [6].



**Table 10** - OpenDSP General Purpose I/O Board ver. 1.1 default DIP-switches settings.

Switch S1	Default setting
1 (Address selection)	OFF
2 (Address selection)	ON
3 (Address selection)	ON
4 (Address selection)	ON
5 (Address selection)	ON
6 (Address selection)	ON
7 (INT sel.)	ON
8 (INT sel.)	OFF
Switch S2	Default setting
1 (INT en.)	OFF
2 (AD Mode)	ON
3 (AD Mode)	OFF
4 (PC)	OFF

## Tests

The tests include mounting tests for the DSP Mother Board and the General Purpose I/O Board, DSP tests, EPP tests and a final overall system test.

### ☒ DSP Mother Board mounting tests

#### ☒ Altera mounting test

**Purpose:** Verify the correct Altera FPGA pin soldering

**Date:** July 1st, 98

**Operator:** AD

**Result:** Passed

#### ☒ DSP mounting test

**Purpose:** Verify the correct DSP mounting

**Date:** July 1st, 98

**Operator:** AD

**Result:** Passed



☒ **EPP mounting test**

**Purpose:** Verify the EPP connection effectiveness

**Date:** July 1st, 98

**Operator:** AD

**Result:** Passed

☒ **Memory test**

**Purpose:** Verify the SRAM and NVRAM memory accessibility

**Date:** July 1st, 98

**Operator:** AD

**Result:** Passed

☒ **I/O Board mounting test**

**Purpose:** Verify the correct Altera FPGA pin soldering

**Date:** July 2nd, 98

**Operator:** AD

**Result:** Passed

☒ **System tests**

**Purpose:** Verify the overall system correct operations

**Date:** July 3rd, 98

**Operator:** AA

**Result:** Passed



## Bibliography

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- [3] Texas Instruments, "TMS320C3x – User's Guide – Digital Signal Processing Solutions", Texas Instruments, U.S.A., July 1997, pp. 8-13/8-42.
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